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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
TSE, YOUNG TOI

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 09/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/241,994	HICKLING, RONALD M.	
	Examiner	Art Unit	
	YOUNG T. TSE	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 7-12 and 14-19 is withdrawn in view of the newly discovered reference(s) to De Vries et al., Ichimura et al., and Reber. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 7-8, 10, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Vries et al. (Newly cited).

De Vries et al. (U.S. Patent No. 5,736,848) discloses a communication system in Fig. 2 for measuring the energy output from one or more electrical energy sources first makes an analog power measurement, and converts the resultant output into digital from.

Referring to Fig. 2, the communication system includes at least an analog power measuring system (1) for inverting a polarity of the input signal u[t], an analog to digital converter (2) including a sigma delta modulator (8) and a digital filter (9) for converting the inverted polarity of the input signal into a series of digital values, and a common

clock (CL 1) for providing a common clock signal to both the analog power measurement system (1) and the sigma delta modulator (8). See column 3, lines 22-35.

Fig. 1 shows the detailed embodiment of the analog power measurement system (1) of Fig. 2. Referring to Fig. 1, the analog power measurement system (1) includes at least a polarity reverser switch (3) including two switch poles for providing the polarity of the input signal through a magnetic field sensor (5) and an amplifier (7). See column 2, line 28 to column 3, line 21.

With respect to claims 1, 7, 10, and 14, the analog power measuring system (1) may consider as a continuous time commutator for inverting the polarity of the input signal u[t] on each clock cycle of the common clock (CL 1) and the sigma delta modulator (8) may consider as the delta-sigma modulator for converting the inverted polarity of the input signal into the series of digital values based on the common clock (CK 1), as recited in the apparatus claims 7 and 14. Also see method claim 1. Further, the digital filter (9) may consider as the programmable digital filter for filtering the series of digital values according to a filter characteristic selected based upon a modulator of the input signal, as recited in claim 10.

Although De Vries et al. does not explicitly show or suggest that the inverted input signal is inverted on every one half clock cycle of the common clock (CK 1). De Vries et al. teaches the polarity reverser (3) consists of a two-polarity commutator in the form of the polarity (3) and whose control input constitutes a clocking input of the analog power measuring system (1) fed the clocking signal (CL 1). The two-pole commutator consists of four on/off switches which are operated by means of two inverters two by

two in push-pull action and thus constitute two single-pole commutators which are commutated synchronously. See column 2, lines 54-64.

De Vries et al. also teaches a two-pole output of the analog power measuring system (1)) is connected to a two-pole input of the sigma-delta modulator (8) with a switching input fed the same clocking signal (CL 1) as the clocking input of the arrangement (1). The sigma-delta modulator (8) contains a polarity reverser (PR in block 8 of Fig. 4) which is commuted periodically by means of the clocking signal (CL 1) in synchronism with the polarity reverser (3) of the arrangement (1) in order to realize polarity commutations. As a consequence, the desired signal is twice polarity-reversed synchronously, once the arrangement (1) and once in the sigma-delta modulator (8). See column 3, lines 24-35.

In other words, when the on/off switches which are operated by means of two inverters two by two in push-pull action and are periodically synchronized with each other. The input signal u[t] is inverted on every one quarter clock cycle, half clock cycle, three quarter clock cycle or full clock cycle.

Therefore, it would have been obvious to one or ordinary skill in the art to provide a clock signal (CL 1) in the polarity reverser (3) of De Vrier's analog power measuring system (1) to produce an inverted input signal which is inverted on every one half clock cycle out of the one quarter clock cycle, the half clock cycle, the three quarter clock cycle, and the full clock cycle.

With respect to claims 4, 8, and 17, the analog power measuring system (1) includes at least the polarity reverser switch (3), the servo amplifiers (4), and the amplifier (7).

4. Claims 2-3, 5-6, 11-12, 15-16, and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Vries et al. in view of Reber (newly cited) as applied to claims 1, 7, and 14.

De Vries et al. fails to show or teach where is the input signal u[t] derived from as recited in claims 2-3, 5-6, 11-12, 15-16, and 18-19.

Reber (U.S. Patent No. 6,393,070 B1) also discloses a similar communication system in Fig. 2 which includes an inverter circuit (12) for inverting the polarity of the input signal (20), a sigma delta modulator (25) for converting the inverted input signal into a series of digital values (26), and a decimation filter for filtering the series of digital values into digital filter values (28).

With respect to claims 2-3, 5-6, 11-12, 15-16, and 18-19, Reber shows a communication device (1) in Fig. 1 wherein the input signal of the inverter circuit (12) is derived from an antenna (3) through an amplifier (2), a first bandpass filter 5, a mixer (6), a second bandpass filter (9), an AGC circuit (10), and a controllable inverter stage (14). As shown in Fig. 1 and Fig. 2, the communication device (1) and the analog to digital converter circuit (11) both are fabricated on a single substrate.

Therefore, it would have been obvious to one of ordinary skill in the are that the source of the input signal in De Vries's inverting circuit and the sigma delta modulator circuit could be derived from a receiver circuit, for example, an antenna circuit and an

aliasing filter to filter a receive signal to prevent aliasing out-of-band signal and noise power into a desired signal band before enter into De Vries's inverting circuit and sigma delta modulator circuit as taught by Reber.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over De Vries et al. in view of Ichimura et al. (Newly cited) as applied to claim 7.

De Vries et al. clearly discloses a continuous time commutator and a sigma delta modulator as recited in claim 7, which are already discussed in claim 7 above. However, De Vries et al. fails to show the detailed embodiment of the sigma-delta modulator (8).

Ichimura et al. (U.S. Patent No. 5,835,042) discloses the detailed embodiment of a sigma-delta modulator (3) in Fig. 3 which includes an adder (11) for adding an input signal (2) from a feedback signal, an integrator (12), a comparator (13), a sample delay (14), and a 1 bit D/A converter (15) for providing the feedback signal to the adder (11).

With respect to claim 9, the integrator (12) may consider as the loop amplifier and the continuous time loop filter; the comparator (13) may consider as the edge-triggered comparator; and the 1 bit D/A converter (15) may consider as the one-bit digital to analog comparator.

Applicant note although Ichimura et al. does not mention the integrator (12) is consisted of a loop amplifier and a loop filter. It is well known to a person skill in the art that a loop amplifier and a loop filter act as an integrator. Also see page 11, lines 8-9 of the instant application.

Therefore, it would be been obvious to one of ordinary skill in the art to include a loop amplifier, a loop filter, a comparator, and a one-bit D/A converter in the sigma-delta modulator (8) of De Vries's communication system as taught by Ichimura et al. in order to overcome the problem of long ladder carry propagation delays or its simplicity and its robustness against circuit imperfections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Young Tse** whose telephone number is **(703) 305-4736**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Stephen Chin**, can be reached at **(703) 305-4714**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Or:

(703) 872-9315 (for amendments after final rejection only, please mark "EXPEDITED PROCEDURE")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Young T. Tse
Primary Examiner
9/10/02